Claims

What is claimed is:

1. A method for modulating a F-N synthesizer in response to applied sequences of in-phase (I) and quadrature (Q) analog modulation signals, said F-N synthesizer comprising a loop divider having a variable fractional divisor, the method comprising

comparing said sequence of I analog modulation signals with a first plurality of threshold values at successive time intervals, thereby to generate a sequence of I digital output signals, said I digital output signals corresponding to respective relationships between said I analog modulation signals and said plurality of thresholds at said successive time intervals,

comparing said sequence of Q analog modulation signals with a second plurality of threshold values at successive time intervals, thereby to generate a sequence of Q digital output signals, said Q digital output signals corresponding to respective relationships between said Q analog modulation signals and said plurality of thresholds at said successive time intervals,

transforming said I and Q digital output signals into a sequence of digital modulation signals in accordance with a predetermined relationship between values of said I and Q digital output signals in consecutive time intervals, and

modifying said variable divisor in accordance with said sequence of digital modulation signals.

2. The method of claim 1wherein

said first plurality of threshold values comprises a threshold value equal to a predetermined function of maximum absolute value of positive peak values for said I analog signals and a threshold value equal to a predetermined function of maximum absolute value of negative peak values for said I analog signals, and

said second plurality of threshold values comprises a threshold value equal to a predetermined function of maximum absolute value of positive peak values for said Q

analog signals and a threshold value equal to a predetermined function of maximum absolute value of negative peak values for said Q analog signals

3. The method of claim 2 wherein

said first plurality of threshold values comprises a value substantially equal to 0.7 times the positive peak value of said I analog signals, and a value substantially equal to 0.7 times the negative peak value of said I analog signals, and

said second plurality of threshold values comprises a value substantially equal to 0.7 times the positive peak value of said Q analog signals, and a value substantially equal to 0.7 times the negative peak value of said Q analog signals.

4. The method of claim 1 wherein

said I digital output signals comprise at least three values,

said Q digital output signals comprise at least three values, and

wherein said predetermined relationship between values of said I digital output signals and said Q digital output signals in consecutive time intervals comprises a predetermined relationship between I and Q digital output signals in two consecutive time intervals.

5. The method of claim 4 wherein said modulation signals are GMSK modulation signals.

6. The method of claim 5 wherein

said at least three values for said I digital output values and said at least three values for said Q digital output values are each represented as +1, 0, and -1, and wherein

for states N and N+1 corresponding to values for said I digital output values and said Q digital output values in respective consecutive time intervals N and N+1, said sequence of digital modulation signals are given by

State N	State N+1	Digital Modulation Signal
I=0,Q=1	I=1,Q=0	-1
I=0,Q=1	I=-1,Q=0	+1
I=1,Q=0	I=0,Q=-1	-1
I=1,Q=0	I=0,Q=1	+1
I=0,Q=-1	I=-1,Q=0	-1
I=0,Q=-1	I=1,Q=0	+1
I=-1,Q=0	I=0,Q=1	-1
I=-1,Q=0	I=0,Q=-1	+1.

7. In a radio transmitter having a fractional-N synthesizer (F-N synthesizer) comprising a loop divider having a variable fractional divisor, a method for generating digital modulation signals in response to input analog modulation signals comprising

comparing said analog modulation signals at a plurality of successive time intervals with at least one predetermined threshold value to derive a sequence of digital values, and

decoding said sequence of digital values to generate a corresponding sequence of digital modulation signals,

modifying said variable divisor in accordance with said digital modulation signals.

8. The method of claim 7 wherein said at least one predetermined threshold value comprises at least one value equal to a predetermined function of a peak value of said analog modulation signals.

9. The method of claim 8 wherein said at least one value equal to a predetermined function of a peak value comprises one positive threshold value equal to a predetermined percentage of a positive peak value of said analog modulation signals and one negative threshold value equal to a predetermined percentage of a negative peak value of said analog modulation signals.

10. The method of claim 9 wherein

a first of said digital values, represented as +1, is achieved when said analog modulation signals exceeds said positive threshold value at a predetermined time,

a second of said digital values, represented as a -1, is achieved when said analog modulation signals are more negative than said negative threshold value at said predetermined time, and

a third of said digital values, represented as a 0, is achieved when neither of said first or second digital values is achieved.

11. The method of claim 7 wherein

said analog signals comprise in-phase (I) signals and quadrature (Q) signals, and

said comparing comprises comparing said I signals and said Q signals separately with respective predetermined threshold values to derive separate sequences of digital values corresponding to each said each of said I and Q analog signals.

12. The method of claim 11 wherein said decoding comprises decoding said separate sequences of digital values corresponding to each of said I and Q analog signals to generate said digital modulation signals.

13. A signal converter comprising

an input circuit for receiving analog modulation signals,

at least one comparator for comparing at least one of said analog modulation signals with at least one threshold signal level to produce a first output digital signal when said at least one analog modulation signal bears a first relationship to said at least one threshold signal level and to produce a second output digital signal when said at least one analog modulation signal bears a second relationship to said at least one threshold signal level,

a decoder for receiving first and second output digital signals from said at least one comparator and outputting digital modulation signals corresponding to said analog modulation signals, and

a divider circuit having a variable fractional divisor determined by said digital modulation signals.

14. The converter of claim 13 wherein said analog modulation signals comprise in-phase (I) and quadrature (Q) signals.

15. The converter of claim 14 wherein said analog modulation signals comprise GMSK analog modulation signals.

16. The converter of claim 14 wherein said at least one threshold signal comprises two threshold signals, a first of which comprises a function of a most positive value of said analog modulation signals, and a second of which comprises a function of a most negative value of said analog modulation signals.

17. The converter of claim 16 wherein said at least one comparator comprises comparators for comparing each of said I and Q analog modulation signals with each of said first and second threshold signals.

18. The converter of claim 17 wherein said comparators provide first output digital signals and second output digital signals corresponding to each of said I and Q analog input signals.

19. The converter of claim 18 wherein said decoder receives said first and second output digital signals corresponding to each of said I and Q analog input signals and outputs digital modulation signals corresponding to both of said I and Q input analog modulation signals.

20. The converter of claim 13 wherein said divider is a loop divider in a fractional-N (F-N) synthesizer.

21. The converter of claim 20 further comprising a switch for applying digital modulation signals from said decoder to said divider.

22. The converter of claim 20 further comprising a switch for applying digital modulation signals to said divider from a source other than said decoder.

23. The converter of claim 20 further comprising a switch for applying digital modulation signals from

said decoder to said divider in response to a first set of control signals, and

a source other than said decoder to said divider in response to a second set of control signals, and wherein

said first and second sets of control signals are mutually exclusive.